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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,190	03/18/2004	Shunpei Yamazaki	0756-7269	5109

31780 7590 02/24/2010

ERIC ROBINSON
PMB 955
21010 SOUTHBANK ST.
POTOMAC FALLS, VA 20165

EXAMINER	
TRAN, MY CHAU T	

ART UNIT	PAPER NUMBER
2629	

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02/24/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

ADVISORY ACTION (CONT.)

Application and Claims Status

1. Applicant's response filed 02/02/2010 are acknowledged and entered.

2. Claims 1-37 were pending. No claims were amended, added, and/or cancelled. Therefore, claims 1-37 are currently pending. Claims 2-5, 8, 9, 12, 13, and 15-22 are drawn to non-elected species and/or inventions, wherein the election was made *with* traverse in the reply filed on 05/16/2007, and thus these claims remain withdrawn from further consideration by the examiner, 37 CFR 1.142(b), there being no allowable generic claim.

Information Disclosure Statement

3. The information disclosure statement filed 02/02/2010 fails to comply with 37 CFR 1.97(d) because it lacks a statement as specified in 37 CFR 1.97(e). It has been placed in the application file, but the information referred to therein has not been considered.

Status of Claim(s) Objection(s) and /or Rejection(s)

4. The rejection of claims 32-37 under 35 USC 112, first paragraph (new matter) has been withdrawn in light of applicant's arguments, see pg. 3, last paragraph, thru pg. 6, lines 1-2, filed 02/02/2010.

Response to Arguments

5. The following rejection(s) and/or objection(s) that have not been withdrawn as indicated above are maintained and the arguments are addressed below.

6. Applicant's arguments directed to the 103(a) rejection were considered but they are not persuasive for the following reasons.

[1] Applicant asserts that the references of Nishitoba et al. and Yamazaki either alone or in combination, do not teach or suggest the claimed limitation of "*"wherein the first transistor and the second transistor share a same semiconductor island, i.e. the first and second transistors are formed on the same semiconductor layer/island*" of independent claims 1, 7, 11, and 23-25.

Thus, the combine references of Nishitoba et al. (US Patent 6,774,877) and Yamazaki (US Patent Application Publication US 2002/0047825 A1) do not render the instant claimed inventions *prima facie* obvious.

This is not found persuasive for the following reasons:

[1] The examiner respectfully disagrees. It is the examiner's position that the combine teachings of Nishitoba et al. and Yamazaki do disclose the claimed limitation of "*wherein the first transistor and the second transistor share a same semiconductor island*" of independent claims 1, 7, 11, and 23-25. First, the limitation of '*the first transistor and the second transistor share a same semiconductor island*' of independent claims 1, 7, 11, and 23-25 would encompass the interpretation that the "*semiconductor island*" is an additional layer on top of a substrate on which "*the first transistor and the second transistor*" are formed. This interpretation is supported by the originally filed specification (see fig. 5) and the originally filed specification does not specifically define

the term "*semiconductor island*" such that it would exclude this interpretation. Here, Yamazaki disclose wherein the entire complete sentence is repeated "***[0044]*** *First, referring to* ***FIG. 1A****, a silicon oxide film as an underlayer film* ***102*** *is formed on a glass substrate and gate electrodes* ***103*** *and* ***104*** *are formed thereon*". This disclosure does suggest the reference of Yamazaki do suggest claimed limitation of "*wherein the first transistor and the second transistor share a same semiconductor island*" of independent claims 1, 7, 11, and 23-25. Second, Yamazaki disclose a ***silicon oxide film*** not silicon oxide as asserted by applicant (i.e. "*As is readily understood to those of ordinary skill in the art, "silicon oxide" is not a semiconductor. "Silicon oxide" is generally an insulator; whereas, a "semiconductor" is semiconductive. As such, a "silicon oxide film" cannot reasonably correspond to a "semiconductor island.*"" as indicated by applicant). A silicon oxide film is art recognized to be a polymeric solid with the repeating monomer of $Si(O)_2$, which has conductive property. The term "*semiconductor*" as define by the dictionary is any of a class of solids (as germanium or silicon) whose electrical conductivity is between that of a conductor and that of an insulator in being nearly as great as that of a metal at high temperatures and nearly absent at low temperatures (a copy is provided of the Merriam-Webster Dictionary of the term '*semiconductor*'). Thus, the silicon oxide film of Yamazaki would encompass the claimed term "*semiconductor island*". Third, applicant has not provide any structural distinction between the instant claimed "*semiconductor island*" and the silicon oxide film of Yamazaki. Moreover, structurally as claimed the "*semiconductor island*" comprises "*the first transistor and the second transistor*". Here, the silicon oxide film of Yamazaki meets this structural feature

wherein the gate electrodes (ref. #103 and 104) of the transistors are formed on the silicon oxide film (see sections: [0043]-[0044]).

Therefore, the combine teachings of Nishitoba et al. and Yamazaki do render the inventions of the instant claims *prima facie* obvious, and the rejection is maintained.

Allowable Subject Matter

7. Claims 32-37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MY-CHAU T. TRAN whose telephone number is 571-272-0810. The examiner can normally be reached on Monday: 8:00-2:30; Tuesday-Thursday: 7:30-5:00; Friday: 8:00-3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard A. Hjerpe can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MY-CHAU T. TRAN/
Primary Examiner, Art Unit 2629

February 24, 2010